Course:Computer Architer For Control Signal Generation

# NAME:S.Harika

# Reg.no:192111602

# Code:CSA1290

## EXP 1: 8 BIT ADDITION

LDA 2050

MOV B,A

LDA 2051

ADD B

STA 2052

HLT

## EXP 2: 16 BIT ADDITION

LHLD 2500

XCHG

LHLD 2501

MOV A,E

ADD L

MOV L,A

MOV A,D

ADC H

MOV H,A

SHLD 2502

### EXP 3:16 BIT SUBTRACTION

LHLD 2500

XCHG

LHLD 2501

MOV A,E

SUB L

MOV L,A

MOV A,D

ADC H

MOV H,A

SHLD 2502

HLT

### EXP 4:8 BIT SUBTRACTION

LDA 2050

MOV B,A

LDA 2052

SUB B

STA 2054

HLT

### EXP 5:8 BIT MULTIPLICTION

MVI D,00

MVI A,00

LXI H,4150

MOV B.,M

INX H

MOV C,M

LOOP: ADD B

JNC NEXT

INR D

NEXT: DCR C

JNZ LOOP

STA 4152

MOV A,D

STA 4153

HLT

### EXP 6:8 BIT DIVISION

LXI H,1100

MOV B,M

MVI C,00

INX H

MOV A,M

LOOP: CMP B

JC SKIP

SUB B

INR C

JMP LOOP

SKIP: STA 1102

MOV A,C

STA 1103

HLT

### EXP 7: HALF ADDER USING LODINSIM